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10/020,034	12/07/2001	Jozef D. Mitros	TI-32931	8951

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EXAMINER
PHAM, LONG

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/020,034	Applicant(s) MITROS ET AL.	
	Examiner Long Pham	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other

Response to Arguments

1. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

1. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US '082) in view of Nakahara (US '242) (a newly cited reference).

Lin teaches a method of fabricating MOSFET transistors in a semiconductor device, comprising (see figures 1, 2A-2F, and 3A-3E and col. 1, line 10 to col.7, line 5):

providing a semiconductor device substrate 200,

implanting a first transistor region associate with a first transistor device (NMOS) 208 in the semiconductor device substrate by a first implantation to adjust a threshold voltage associated with the first transistor device;

implanting a portion of a second transistor region associated with a second transistor device (PMOS) 210 in the semiconductor device substrate to form a source/drain region 250 associated with the second transistor device by a second implantation;

forming a first gate oxide structure 204a having a first thickness overlying a channel region in the first transistor region;

forming a second gate oxide structure 204b having a second thickness overlying a channel region of the second transistor region, the second thickness being greater than the first thickness;

implanting a portion of the first transistor region to form a source/drain region associated with the first transistor device using a third implantation.

implanting a third transistor region associated with a third transistor device (NMOS) 212 in the semiconductor device by a fourth implantation to adjust a threshold voltage associated with the third transistor device;

implanting a portion of a fourth transistor region associated with a fourth source/drain region associated with the fourth transistor device by fifth implantation;

forming a third gate oxide structure 204a having a third thickness overlying a channel region in the third transistor region;

forming a fourth gate oxide structure having a fourth thickness overlying a channel region in the fourth transistor region, the fourth thickness being greater than the third thickness;

implanting a portion of the third transistor region to form a source/drain region associated with the third transistor device by sixth implantation;

With respect to claims 6 and 16, the use of phosphorus in forming threshold voltage and source/drain region is well-known to ***one of ordinary skill in the art of making semiconductor devices***.
With respect to claim 7, Lin fails to teach the implantation energy and dose for the threshold voltage and source/drain region implants.
However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal value for the implantation energy and dose for the threshold voltage and source/drain region implants through routine experimentation and optimization to obtain optimal or desired device performance because the implantation energy and dose for the threshold voltage and source/drain region implants are a result-effective variables and there is no evidence indicating that the implantation energy and dose for the threshold voltage and source/drain region implants are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.
Further with respect to claim 7, Lin teaches doing the punch-through implantations in the third and fourth transistor devices but fails to teach the implantation energy and dose for the punch-through implantations.
However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal value for the implantation energy and dose for the punch-through implantations through routine experimentation and optimization to obtain optimal or desired device performance because the implantation energy and dose for the punch-through implantations are a result-effective variables and there is no evidence indicating that the implantation energy and dose for the punch-through implantations are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

[illegible] voltage and source/drain region is well-known to ***one of ordinary skill in the art of making semiconductor devices***.
With respect to claims 9, 11, 13, and 17, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal value for the implantation energy and dose through routine experimentation and optimization to obtain optimal or desired device performance because the implantation energy and dose are a result-effective variables and there is no evidence indicating that the implantation energy and dose are critical and it has been held that it is not inventive to discover the

optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 10, the use of arsenic in forming threshold voltage and source/drain region is well-known to ***one of ordinary skill in the art of making semiconductor devices***.

Lin teaches that the first gate oxide structures has a first thickness and the second gate oxide structures has a second thickness but fails to the values for the first and second thicknesses as recited in present claims 14 and 15. However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal value for the thicknesses for the first and second gate oxide structures through routine experimentation and optimization to obtain optimal or desired device performance because the thicknesses for the first and second gate oxide structures are result-effective variables and there is no evidence indicating that the thicknesses for the first and second gate oxide structures are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Lin teaches that the threshold voltage region of the first transistor device and the source/drain or LDD region of the second transistor device are formed by two separate implantation processes but fails to teach that the threshold voltage region of the first transistor device and the source/drain or LDD region of the second transistor device are formed by a single implantation process or simultaneously as recited in present claim 1.

Nakahar teaches a process of forming multiple MOS devices on a substrate in which the threshold voltage region of a MOS device and the source/drain regions of another MOS device are formed simultaneously by implantation. See figures 1A-1E and 2A-2B, 3, and 4 and col. 1, line 5 to col. 6, line 55. It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to form the threshold voltage region of the first

device simultaneously or in a single implantation step in Lin's method because in doing so high-speed MOS devices can be obtained. See col. 1, lines 54-60.

Lin teaches that the threshold voltage region of the third transistor device and the source/drain or LDD region of the fourth transistor device are formed by two separate implantation processes but fails to teach that the threshold voltage region of the third transistor device and the source/drain or LDD region of the fourth transistor device are formed simultaneously or by a single implantation process as recited in present claim 3.

Nakahar teaches a process of forming multiple MOS devices on a substrate in which the threshold voltage region of a MOS device and the source/drain regions of another MOS device are formed simultaneously by implantation. See figures 1A-1E and 2A-2B, 3, and 4 and col. 1, line 5 to col. 6, line 55. It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to form the threshold voltage region of the third transistor device and the source/drain or LDD region of the fourth transistor device simultaneously or in a single implantation step in Lin's method because in doing so high-speed MOS devices can be obtained. See col. 1, lines 54-60.

2. Claims 18, 19, 20, 21, 22, 23, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US '082) in view of Nakahara (US '242) (a newly cited reference).

Lin teaches a method of fabricating MOSFET transistors in a semiconductor device, comprising (see figures 1, 2A-2F, and 3A-3E and col. 1, line 10 to col.7, line 5):

adjusting a threshold voltage 226 of a first transistor device 208 (NMOS) by a first implantation process;

forming a source/drain region 250 of a second transistor device 210 (PMOS) by a second implantation process, wherein the forming of the source/drain region further comprises forming a LDD region of the second transistor device;

forming a first gate oxide structure 204a of the first transistor device having a first thickness;

forming a second gate oxide structure 204b of the second transistor device having a second thickness, the second thickness being greater than the first thickness;

adjusting a threshold voltage 218 of a third transistor device 206 (PMOS) by third implantation process;

forming a source/drain region 250 of a fourth transistor device 210 (PMOS) by a fourth implantation process, wherein the forming of the source/drain region further comprises forming a LDD region of the fourth transistor device.

Lin teaches that the threshold voltage region of the first transistor device and the source/drain or LDD region of the second transistor device are formed by two separate implantation processes but fails to teach that the threshold voltage region of the first transistor device and the source/drain or LDD region of the second transistor device are formed by a single implantation process or simultaneously as recited in present claim 18.

Nakahar teaches a process of forming multiple MOS devices on a substrate in which the threshold voltage region of a MOS device and the source/drain regions of another MOS device are formed simultaneously by implantation. See figures 1A-1E and 2A-2B, 3, and 4 and col. 1, line 5 to col. 6, line 55. It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to form the threshold voltage region of the first transistor device and the source/drain or LDD region of the second transistor device simultaneously or in a single implantation step in Lin's method because in doing so high-speed MOS devices can be obtained. See col. 1, lines 54-60.

Lin teaches adjusting the threshold voltage 226 of the first transistor device 208 using boron but fails to teach that the source/drain or LDD region is formed using boron ion as recited in present claim 24.

However, the use of boron in forming source/drain or LDD region of the MOS device is well-known to ***one of ordinary skill in the art of making semiconductor devices***.

Lin teaches adjusting the threshold voltage 226 of the third transistor device 208 using phosphorus but fails to teach that the source/drain or LDD region is formed using phosphorus ion as recited in present claim 25.

However, the use of phosphorus in forming source/drain or LDD region of the MOS device is well-known to ***one of ordinary skill in the art of making semiconductor devices***.

3. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US '082) in view of Nakahara (US '242) (a newly cited reference).

Lin teaches a method of forming a source/drain region in a semiconductor device, comprising (see figures 1, 2A-2F, and 3A-3E and col. 1, line 10 to col.7, line 5):

implanting a first transistor region using boron or phosphorus to adjust a threshold voltage associated with the first transistor device 208 by a first implantation process; and

to form a source/drain region 250 associated with a second transistor device 212 by a second implantation process.

Lin teaches that the threshold voltage region of the first transistor device and the source/drain of the second transistor device are formed by two separate implantation processes but fails to teach that the threshold voltage region of the first transistor device and the source/drain region of the second transistor device are formed by a single implantation process as recited in present claim 26.

Nakahar teaches a process of forming multiple MOS devices on a substrate in which the threshold voltage region of a MOS device and the source/drain regions of another MOS device are formed simultaneously by implantation. See figures 1A-1E and 2A-2B, 3, and 4 and col. 1, line 5 to col. 6, line 55. It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to form the threshold voltage region of the first transistor device and the source/drain or LDD region of the second transistor device simultaneously or in a single implantation step in Lin's method because in doing so high-speed MOS devices can be obtained. See col. 1, lines 54-60.

4. Claims 28, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US '082) in view of Nakahara (US '242) (a newly cited reference).

Lin teaches a method of fabricating a semiconductor device, comprising (see figures 1, 2A-2F, and 3A-3E and col. 1, line 10 to col.7, line 5):
implanting an active region of a low voltage NMOS device 208 (thinner gate oxide implies low voltage) by a first implantation of boron;
implanting source/drain regions of a high voltage PMOS device 210 (thicker gate oxide implies high voltage) by a second implantation;
implanting an active region of a low voltage PMOS device 206 by a third implantation of phosphorus;
implanting source/drain regions of a high voltage NMOS device 212 by a fourth implantation;
forming polysilicon gate structures 246 associated with the high and low voltage NMOS and PMOS devices;
forming sidewall spacers 248 on opposite sides of the polysilicon gate structures;
forming a first gate oxide structure 204a over the low voltage NMOS and PMOS devices having a first thickness;
forming a second gate oxide structure 204b over the high voltage NMOS and

greater than the first thickness;
implanting source/drain regions associated with the low voltage NMOS device by a fifth implantation; and
implanting source/drain regions associated with the low voltage PMOS device by a sixth implantation.
Lin teaches that the threshold voltage or active region of the low voltage NMOS device and the source/drain or LDD region of the high voltage PMOS device are formed by two separate implantation processes but fails to teach that the threshold voltage region of the low voltage NMOS device and the

source/drain or LDD region of the high voltage PMOS device are formed by a single implantation process as recited in present claim 28.
Nakahar teaches a process of forming multiple MOS devices on a substrate in which the threshold voltage region of a MOS device and the source/drain regions of another MOS device are formed simultaneously by implantation. See figures 1A-1E and 2A-2B, 3, and 4 and col. 1, line 5 to col. 6, line 55.
It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to form the threshold voltage region of the first transistor device and the source/drain or LDD region of the second transistor device simultaneously or in a single implantation step in Lin's method because in doing so high-speed MOS devices can be obtained. See col. 1, lines 54-60.
Lin teaches that the threshold voltage or active region of the low voltage PMOS device and the source/drain or LDD region of the high voltage NMOS device are formed by two separate implantation processes but fails to teach that the threshold voltage region of the low voltage PMOS device and the source/drain or LDD region of the high voltage NMOS device are formed by a single implantation process as recited in present claim 28.
Nakahara teaches a process of forming multiple MOS devices on a substrate in which the threshold voltage region of a MOS device and the source/drain regions of another MOS device are formed simultaneously by implantation. See figures 1A-1E and 2A-2B, 3, and 4 and col. 1, line 5 to col. 6, line 55.
It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to form the threshold voltage region of the first transistor device and the source/drain or LDD region of the second transistor device simultaneously or in a single implantation step in Lin's method because in doing so high-speed MOS devices can be obtained. See col. 1, lines 54-60.
Lin teaches adjusting the threshold voltage 226 of the low voltage NMOS device using boron but fails to teach that the source/drain or LDD regions of [illegible] formed using boron ion as recited in present claim 28.
However, the use of boron in forming source/drain or LDD region of the MOS device is well-known to ***one of ordinary skill in the art of making semiconductor devices***.
Lin teaches adjusting the threshold voltage of the low voltage PMOS device using phosphorus but fails to teach that the source/drain or LDD regions of the high voltage NMOS device are formed using phosphorus ion as recited in present claim 28.

However, the use of phosphorus in forming source/drain or LDD region of the MOS device is well-known to ***one of ordinary skill in the art of making semiconductor devices***.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4082 for regular communications and 703-746-4082 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Long Pham
Primary Examiner
Art Unit 2823

L. P.
September 10, 2002